Release Notes

Intel® Platform Controller Hub (PCH) Chipset Initialization (Chipset_Init) Format 2.0

- Tiger Lake UP3 and UP4

Date: May 11, 2020

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Platform Support:

The latest Intel® Platform Controller Hub (PCH) Chipset Initialization (Chipset_Init) Format 2.0 binary file supports the following:

- TglPchLpChipsetInitZ0V5.bin= Tiger Lake PCH-LP Z0
- TglPchLpChipsetInitA0V11.bin= Tiger Lake PCH-LP A0

REVISION HISTORY:

Binary File	PCH SKU	PCH Stepping Identifier (yy)	Chipset_Init Version Hex (Dec)	Description
TglPchLpChipsetInitZ0V4	Z0	0xF0	0x04 (4)	Initial Release for Z0
TglPchLpChipsetInitZ0V5	Z0	0xF0	0x05 (5)	V4 incorporated incorrect OPI-DMI PHY Mode register setting. V5 writes the correct OPI-DMI PHY Mode register setting value
TglPchLpChipsetInitA0V8	A0	0x00	0x08 (8)	Initial Release for A0
TglPchLpChipsetInitA0V10	A0	0x00	0x0A (10)	• Incorporates updated Modular PHY (ModPHY) PCH PCIe* Gen1 Rx L0s settings for improved margins • Incorporates latest OPI-DMI PHY Mode recipe Revision 3.0
TglPchLpChipsetInitA0V11	A0	0x00	0x0B (11)	Incorporates updated Modular PHY (ModPHY) recipe revision 9p08